Back End Electronics in LAr Phase-II Upgrade

BROOKHAVEN NATIONAL LABORATORY

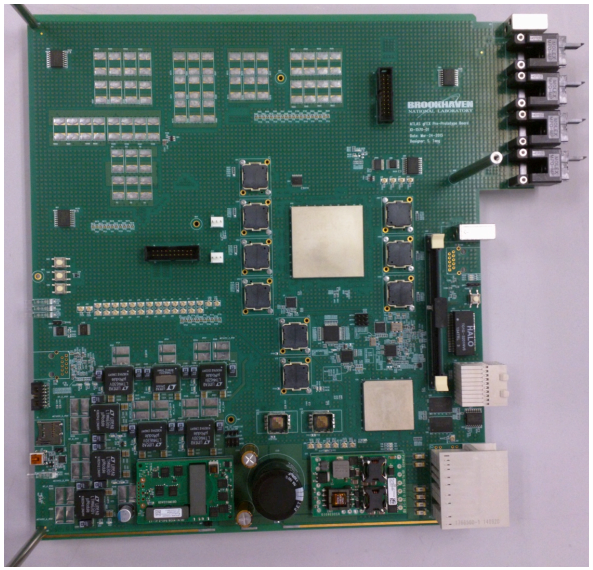
Outline

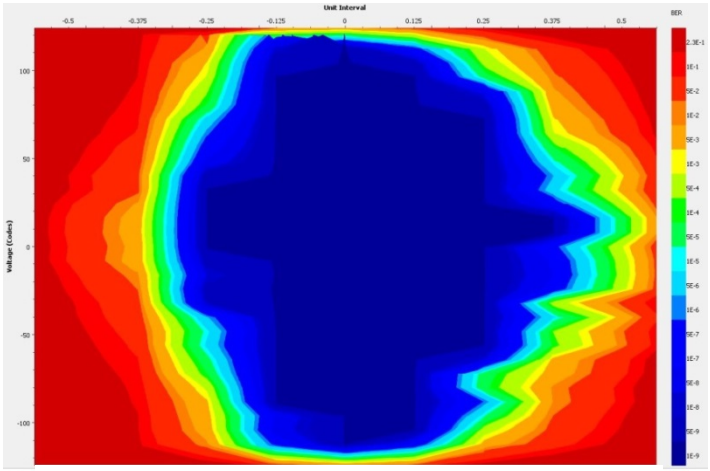
- BNL's Interests
- Proposed BNL's Contribution
- Resources

BNL's Interests

- BNL has been working on the R&D of BE electronics for LAr upgrade since 2005
- Focused on key technologies to enable the breakthrough and optimized system architecture for overall LAr readout and trigger readout electronics systems
  - High speed parallel optical links
  - High performance FPGA with high speed transceivers and high speed DSP
  - Industrial standard platform (ATCA) to house the new BE electronics system
  - Modular design (AMC) to ease the development and make efficient use of expertise from collaboration
  - Close collaboration with US universities (UAZ, SBU) and other international LAr institutes
    - First ATCA module with UAZ in 2008/09
    - Development of AMC module with SBU in 2012/13

BNL's Interests





Processor FPGA/MiniPODs link at 12.8 Gb/s
-3 FPGA with 13.1Gb/s GTH

- FMC MicroPOD Mezzanine
  - Evaluation of both MicroPOD and custom cooling solution
  - First demonstration of non-symmetrical transceiver speeds in FPGA
- Joint BNL/RAL 10Gb/s Link Test in 2013
  - Characterization test of > 10Gbps parallel optical links
  - Enable the > 6.4 Gb/s link speed interface between LAr and L1Calo, currently 11.2 Gb/s
- This has been documented LAr Phase-I Upgrade TDR
  - Important to the ATLAS LAr Phase-I upgrade project and also the US responsibility of BE electronics in USATLAS Phase-I construction project
- Recently gFEX pre-prototype demonstrated 80 links running at 12.8Gbps simultaneously

Proposed BNL's Contribution

- Evaluation and development of key technologies
  - High speed parallel optical links
    - > 25Gbps parallel optical transceivers – CFP4, QSFP28, Firefly, Duplex MiniPOD
  - High performance FPGA with high speed transceivers and high speed DSP
    - Xilinx Ultrascale & Ultrascale+ FPGA
  - BNL was responsible of BE high speed data transmission in USATLAS Phase-I construction project in FY14
- Development of LPPR (Liquid Argon Pre-Processor) to interface to LFEB in front end and L1Global/FELIX in TDAQ
  - Focus on board design with FPGA and optical transceivers
    - Recent experience: gFEX & PCIe card for LTDB test
  - Contribute to the firmware development
    - Recent experience: GBT firmware for FELIX, and infrastructure firmware (link & parallel bus) for gFEX

Resources

- R&D Phase
  - BNL can contribute 0.5 FTE EE per year for BE electronics in USATLAS LAr Phase-II upgrade
- Construction Phase
  - BNL can contribute 2 FTE EE per year for BE electronics in USATLAS LAr Phase-II construction project
- Proposed Tasks
  - Lead the design and integration of LPPR, with focus on the high speed parallel optical links and high performance FPGA
  - Contribute to the firmware development of LPPR
  - Work closely with university groups
  - Involvement will be determined by the overall plan of USATLAS Phase-II upgrade